# DDR2 Unbuffered SODIMM

## 200pin Unbuffered SODIMM based on 512Mb B-die

## 64bit Non-ECC

## DDR2 Unbuffered SODIMM Ordering Information

| Part Number | Density | Organization | Component Composition | Number of Rank | Height |
|---|---|---|---|---|---|
| M470T3354BG(Z)3-CD5/CC | 256MB | 32Mx64 | 32Mx16(K4T51163QB)*4 | 1 | 30mm |
| M470T3354BG(Z)0-CD5/CC | 256MB | 32Mx64 | 32Mx16(K4T51163QB)*4 | 1 | 30mm |
| M470T3354BZ3-LD5/CC | 256MB | 32Mx64 | 32Mx16(K4T51163QB)*4 | 1 | 30mm |
| M470T3354BZ0-LD5/CC | 256MB | 32Mx64 | 32Mx16(K4T51163QB)*4 | 1 | 30mm |
| M470T6554BG(Z)3-CD5/CC | 512MB | 64Mx64 | 32Mx16(K4T51163QB)*8 | 2 | 30mm |
| M470T6554BG(Z)0-CD5/CC | 512MB | 64Mx64 | 32Mx16(K4T51163QB)*8 | 2 | 30mm |
| M470T6554BZ3-LD5/CC | 512MB | 64Mx64 | 32Mx16(K4T51163QB)*8 | 2 | 30mm |
| M470T6554BZ0-LD5/CC | 512MB | 64Mx64 | 32Mx16(K4T51163QB)*8 | 2 | 30mm |
| M470T2953BS(Y)3-CD5/CC | 1GB | 128Mx64 | 64Mx8(K4T51083QB)*16 | 2 | 30mm |
| M470T2953BS(Y)0-CD5/CC | 1GB | 128Mx64 | 64Mx8(K4T51083QB)*16 | 2 | 30mm |
| M470T2953BY3-LD5/CC | 1GB | 128Mx64 | 64Mx8(K4T51083QB)*16 | 2 | 30mm |
| M470T2953BY0-LD5/CC | 1GB | 128Mx64 | 64Mx8(K4T51083QB)*16 | 2 | 30mm |

Note: "Z" and "Y" of Part number(11th digit) stand for Lead-free products.
Note: "3" of Part number(12th digit) stand for Dummy Pad PCB products.

## Features

- Performance range

|  | D5(DDR2-533) | CC(DDR2-400) | Unit |
|---|---|---|---|
| Speed@CL3 | 400 | 400 | Mbps |
| Speed@CL4 | 533 | 400 | Mbps |
| CL-tRCD-tRP | 4-4-4 | 3-3-3 | CK |

- JEDEC standard 1.8V ± 0.1V Power Supply

- $V_{DDQ}$ = 1.8V ± 0.1V

- 200 MHz $f_{CK}$ for 400Mb/sec/pin, 267MHz $f_{CK}$ for 533Mb/sec/pin

- 4 Banks

- Posted $\overline{CAS}$

- Programmable $\overline{CAS}$ Latency: 3, 4, 5

- Programmable Additive Latency: 0, 1 , 2 , 3 and 4

- Write Latency(WL) = Read Latency(RL) -1

- Burst Length: 4 , 8(Interleave/nibble sequential)

- Programmable Sequential / Interleave Burst Mode

- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)

- Off-Chip Driver(OCD) Impedance Adjustment

- On Die Termination

- Average Refresh Period 7.8us at lower than a $T_{CASE}$ 85°C, 3.9us at 85°C < $T_{CASE}$ ≤ 95 °C
  - support High Temperature Self-Refresh rate enable feature

- Package: 60ball FBGA - 64Mx8 , 84ball FBGA - 32Mx16

- All of Lead-free products are compliant for RoHS

Note: For detailed DDR2 SDRAM operation, please refer to Samsung's Device operation & Timing diagram.

## Address Configuration

| Organization | Row Address | Column Address | Bank Address | Auto Precharge |
|---|---|---|---|---|
| 64Mx8(512Mb) based Module | A0-A13 | A0-A9 | BA0-BA1 | A10 |
| 32Mx16(512Mb) based Module | A0-A12 | A0-A9 | BA0-BA1 | A10 |

## Pin Configurations (Front side/Back side)

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{REF}$ | 2 | $V_{SS}$ | 51 | DQS2 | 52 | DM2 | 101 | A1 | 102 | A0 | 151 | DQ42 | 152 | DQ46 |
| 3 | $V_{SS}$ | 4 | DQ4 | 53 | $V_{SS}$ | 54 | $V_{SS}$ | 103 | $V_{DD}$ | 104 | $V_{DD}$ | 153 | DQ43 | 154 | DQ47 |
| 5 | DQ0 | 6 | DQ5 | 55 | DQ18 | 56 | DQ22 | 105 | A10/AP | 106 | BA1 | 155 | $V_{SS}$ | 156 | $V_{SS}$ |
| 7 | DQ1 | 8 | $V_{SS}$ | 57 | DQ19 | 58 | DQ23 | 107 | BA0 | 108 | $\overline{RAS}$ | 157 | DQ48 | 158 | DQ52 |
| 9 | $V_{SS}$ | 10 | DM0 | 59 | $V_{SS}$ | 60 | $V_{SS}$ | 109 | $\overline{WE}$ | 110 | $\overline{S0}$ | 159 | DQ49 | 160 | DQ53 |
| 11 | $\overline{DQS0}$ | 12 | $V_{SS}$ | 61 | DQ24 | 62 | DQ28 | 111 | $V_{DD}$ | 112 | $V_{DD}$ | 161 | $V_{SS}$ | 162 | $V_{SS}$ |
| 13 | DQS0 | 14 | DQ6 | 63 | DQ25 | 64 | DQ29 | 113 | $\overline{CAS}$ | 114 | ODT0 | 163 | NC, TEST | 164 | CK1 |
| 15 | $V_{SS}$ | 16 | DQ7 | 65 | $V_{SS}$ | 66 | $V_{SS}$ | 115 | NC/$\overline{S1}$ | 116 | A13 | 165 | $V_{SS}$ | 166 | $\overline{CK1}$ |
| 17 | DQ2 | 18 | $V_{SS}$ | 67 | DM3 | 68 | $\overline{DQS3}$ | 117 | $V_{DD}$ | 118 | $V_{DD}$ | 167 | $\overline{DQS6}$ | 168 | $V_{SS}$ |
| 19 | DQ3 | 20 | DQ12 | 69 | NC | 70 | DQS3 | 119 | NC/ODT1 | 120 | NC | 169 | DQS6 | 170 | DM6 |
| 21 | $V_{SS}$ | 22 | DQ13 | 71 | $V_{SS}$ | 72 | $V_{SS}$ | 121 | $V_{SS}$ | 122 | $V_{SS}$ | 171 | $V_{SS}$ | 172 | $V_{SS}$ |
| 23 | DQ8 | 24 | $V_{SS}$ | 73 | DQ26 | 74 | DQ30 | 123 | DQ32 | 124 | DQ36 | 173 | DQ50 | 174 | DQ54 |
| 25 | DQ9 | 26 | DM1 | 75 | DQ27 | 76 | DQ31 | 125 | DQ33 | 126 | DQ37 | 175 | DQ51 | 176 | DQ55 |
| 27 | $V_{SS}$ | 28 | $V_{SS}$ | 77 | $V_{SS}$ | 78 | $V_{SS}$ | 127 | $V_{SS}$ | 128 | $V_{SS}$ | 177 | $V_{SS}$ | 178 | $V_{SS}$ |
| 29 | $\overline{DQS1}$ | 30 | CK0 | 79 | CKE0 | 80 | NC/CKE1 | 129 | $\overline{DQS4}$ | 130 | DM4 | 179 | DQ56 | 180 | DQ60 |
| 31 | DQS1 | 32 | $\overline{CK0}$ | 81 | $V_{DD}$ | 82 | $V_{DD}$ | 131 | DQS4 | 132 | $V_{SS}$ | 181 | DQ57 | 182 | DQ61 |
| 33 | $V_{SS}$ | 34 | $V_{SS}$ | 83 | NC | 84 | NC | 133 | $V_{SS}$ | 134 | DQ38 | 183 | $V_{SS}$ | 184 | $V_{SS}$ |
| 35 | DQ10 | 36 | DQ14 | 85 | BA2 | 86 | NC | 135 | DQ34 | 136 | DQ39 | 185 | DM7 | 186 | $\overline{DQS7}$ |
| 37 | DQ11 | 38 | DQ15 | 87 | $V_{DD}$ | 88 | $V_{DD}$ | 137 | DQ35 | 138 | $V_{SS}$ | 187 | $V_{SS}$ | 188 | DQS7 |
| 39 | $V_{SS}$ | 40 | $V_{SS}$ | 89 | A12 | 90 | A11 | 139 | $V_{SS}$ | 140 | DQ44 | 189 | DQ58 | 190 | $V_{SS}$ |
| 41 | $V_{SS}$ | 42 | $V_{SS}$ | 91 | A9 | 92 | A7 | 141 | DQ40 | 142 | DQ45 | 191 | DQ59 | 192 | DQ62 |
| 43 | DQ16 | 44 | DQ20 | 93 | A8 | 94 | A6 | 143 | DQ41 | 144 | $V_{SS}$ | 193 | $V_{SS}$ | 194 | DQ63 |
| 45 | DQ17 | 46 | DQ21 | 95 | $V_{DD}$ | 96 | $V_{DD}$ | 145 | $V_{SS}$ | 146 | $\overline{DQS5}$ | 195 | SDA | 196 | $V_{SS}$ |
| 47 | $V_{SS}$ | 48 | $V_{SS}$ | 97 | A5 | 98 | A4 | 147 | DM5 | 148 | DQS5 | 197 | SCL | 198 | SA0 |
| 49 | $\overline{DQS2}$ | 50 | NC | 99 | A3 | 100 | A2 | 149 | $V_{SS}$ | 150 | $V_{SS}$ | 199 | $V_{DD}$SPD | 200 | SA1 |

Note : NC = No Connect; NC, TEST(pin 163)is for bus analysis tool and is not connected on normal memory modules.

## Pin Description

| Pin Name | Function | Pin Name | Function |
|---|---|---|---|
| CK0,CK1 | Clock Inputs, positive line | SDA | SPD Data Input/Output |
| $\overline{CK0},\overline{CK1}$ | Clock Inputs, negative line | SA1,SA0 | SPD address |
| CKE0,CKE1 | Clock Enables | DQ0~DQ63 | Data Input/Output |
| $\overline{RAS}$ | Row Address Strobe | DM0~DM7 | Data Masks |
| $\overline{CAS}$ | Column Address Strobe | DQS0~DQS7 | Data strobes |
| $\overline{WE}$ | Write Enable | $\overline{DQS0}$~$\overline{DQS7}$ | Data strobes complement |
| $\overline{S0},\overline{S1}$ | Chip Selects | TEST | Logic Analyzer specific test pin (No connect on So-DIMM) |
| A0~A9, A11~A13 | Address Inputs | $V_{DD}$ | Core and I/O Power |
| A10/AP | Address Input/Autoprecharge | $V_{SS}$ | Ground |
| BA0,BA1 | SDRAM Bank Address | $V_{REF}$ | Input/Output Reference |
| ODT0,ODT1 | On-die termination control | $V_{DD}$SPD | SPD Power |
| SCL | Serial Presence Detect(SPD) Clock Input | NC | Spare pins, No connect |

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## Input/Output Functional Description

| Symbol | Type | Function |
|---|---|---|
| CK0-CK1<br>$\overline{CK0}$-$\overline{CK1}$ | Input | The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$ . A Delay Locked Loop (DLL) circuit is driven from the clock input and output timing for read operations is synchronized to the input clock. |
| CKE0-CKE1 | Input | Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low, By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode. |
| $\overline{S0}$-$\overline{S1}$ | Input | Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$, Rank 1 is selected by $\overline{S1}$. Ranks are also called "Physical banks". |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Input | When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM. |
| BA0~BA1 | Input | Selects which DDR2 SDRAM internal bank is activated. |
| ODT0~ODT1 | Input | Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM Extended Mode Register Set (EMRS). |
| A0~A9,<br>A10/AP,<br>A11~A13 | Input | During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be pecharged regardiess of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge. |
| DQ0~DQ63 | In/Out | Data Input/Output pins. |
| DM0~DM7 | Input | The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. |
| DQS0~DQS7<br>$\overline{DQS0}$~$\overline{DQS7}$ | In/Out | The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$ If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately. |
| $V_{DD}$,$V_{DD}$<br>SPD,$V_{SS}$ | Supply | Power supplies for core, I/O, Serial Presence Detect, and ground for the module. |
| SDA | In/Out | This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to $V_{DD}$ to act as a pull up. |
| SCL | Input | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to $V_{DD}$ to act as a pull up. |
| SA0~SA1 | Input | Address pins used to select the Serial Presence Detect base address. |
| TEST | In/Out | The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules(SO-DIMMs). |

## Functional Block Diagram: 512MB, 64Mx64 Module (Populated as 2 rank of x16 DDR2 SDRAMs)
## M470T6554BG(Z)3/M470T6554BG(Z)0
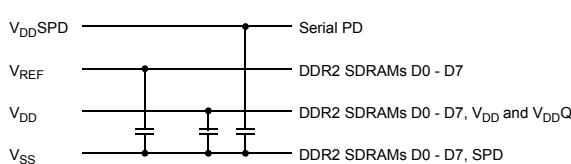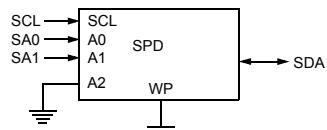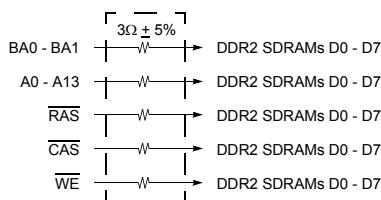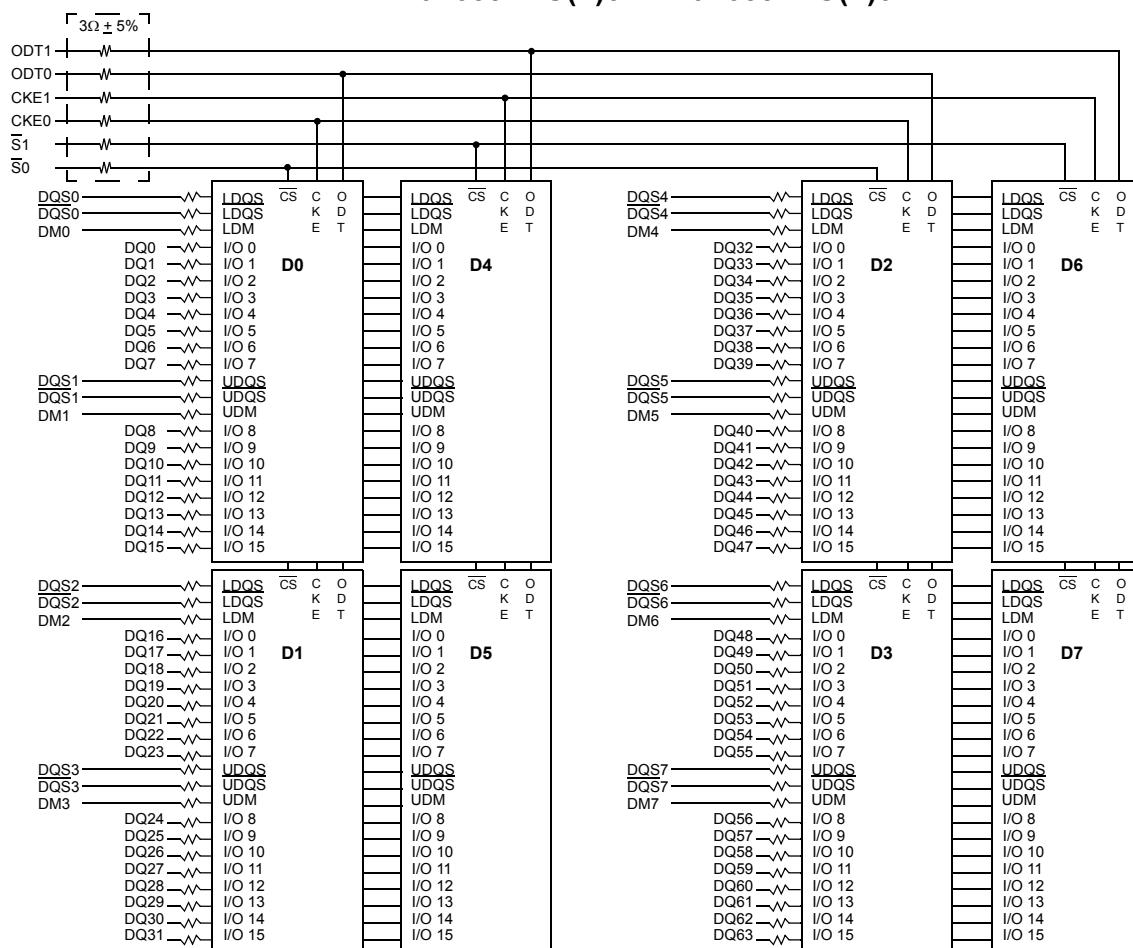


| * Clock Wiring | |
|---|---|
| Clock Input | DDR2 SDRAMs |
| *CK0/$\overline{CK0}$ | 4 DDR2 SDRAMs |
| *CK1/$\overline{CK1}$ | 4 DDR2 SDRAMs |

* Wire per Clock Loading
Table/Wiring Diagrams

Notes :
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 3.0 Ohms ± 5%.

## Functional Block Diagram: 256MB, 32Mx64 Module (Populated as 1 rank of x16 DDR2 SDRAMs)
### M470T3354BG(Z)3/M470T3354BG(Z)0
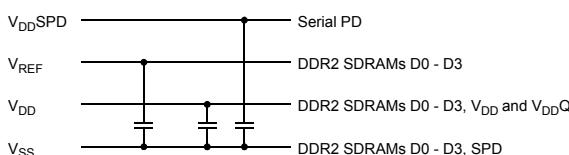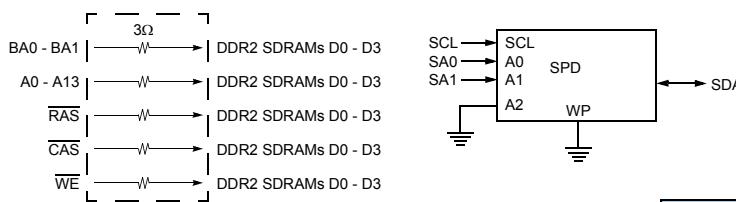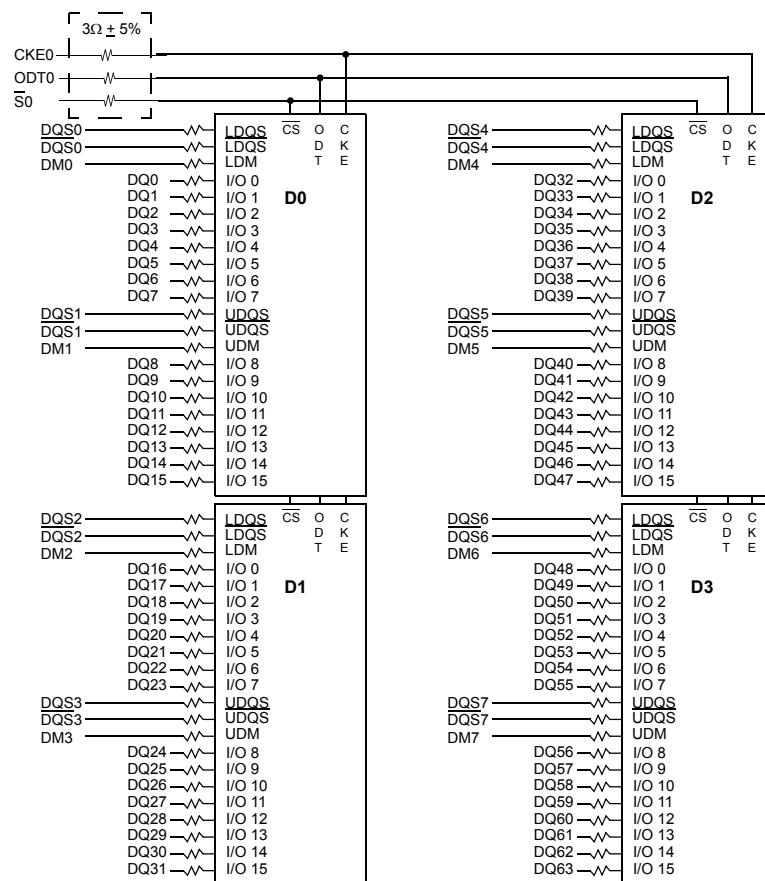


| * Clock Wiring | |
|---|---|
| Clock Input | DDR2 SDRAMs |
| *CK0/$\overline{CK0}$ | 2 DDR2 SDRAMs |
| *CK1/$\overline{CK1}$ | 2 DDR2 SDRAMs |

* Wire per Clock Loading Table/Wiring Diagrams

**Notes :**
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms $\pm$ 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 3.0 Ohms $\pm$ 5%.

## Functional Block Diagram: 1GB, 128Mx64 Module (Populated as 2 ranks of x8 DDR2 SDRAMs)
### M470T2953BS(Y)3/M470T2953BS(Y)0
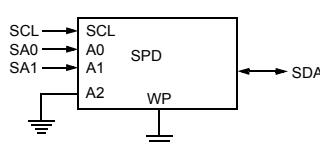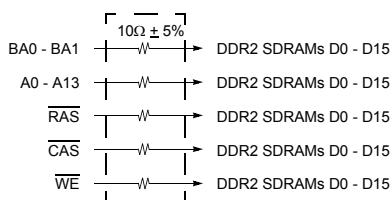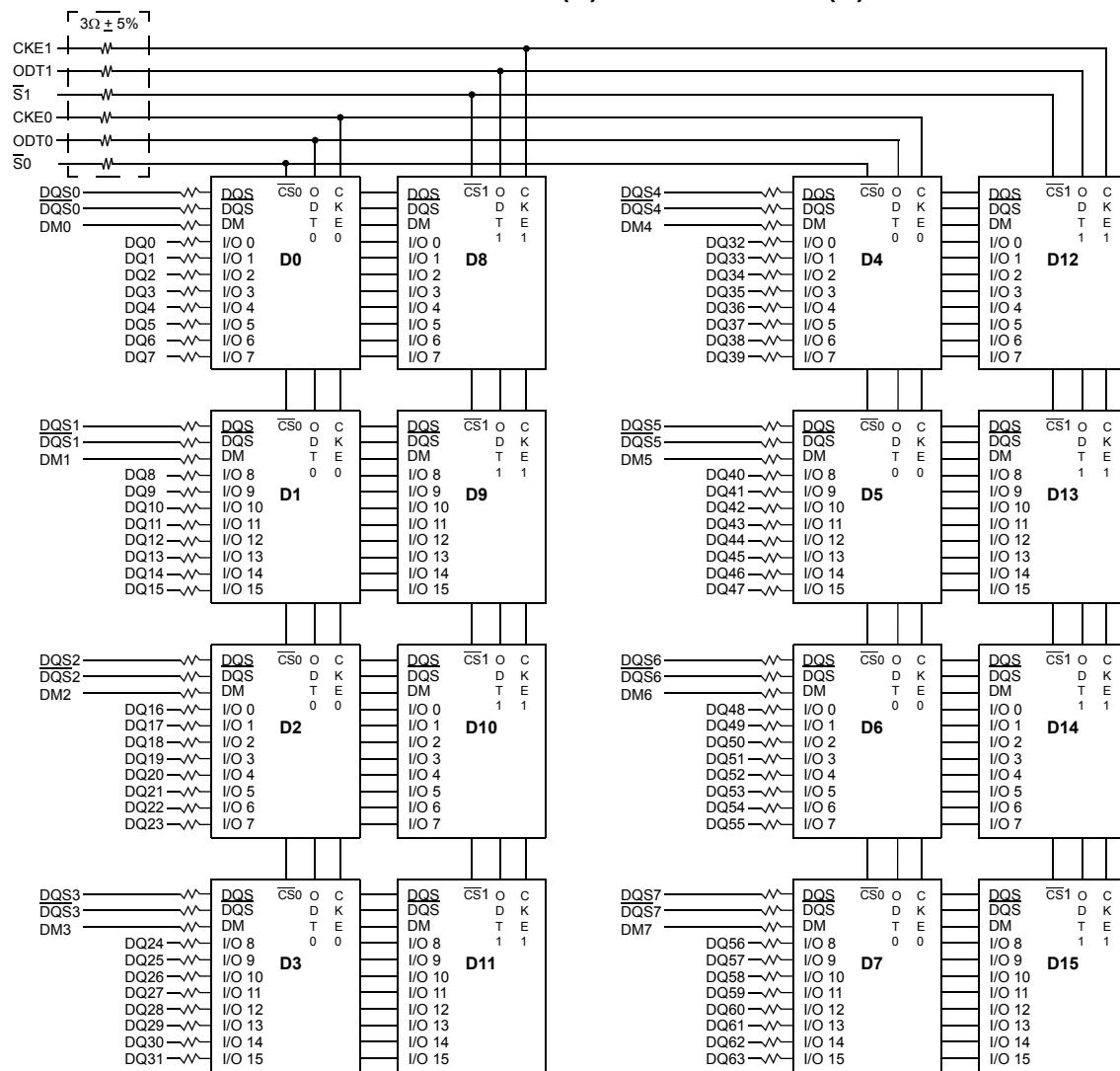


| * Clock Wiring | |
|---|---|
| Clock Input | DDR2 SDRAMs |
| *CK0/$\overline{CK0}$ | 8 DDR2 SDRAMs |
| *CK1/$\overline{CK1}$ | 8 DDR2 SDRAMs |

* Wire per Clock Loading
Table/Wiring Diagrams
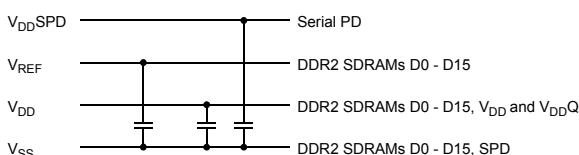
**Notes :**
1. DQ,DM, $\overline{DQS/DQS}$ resistors : 22 Ohms $\pm$ 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 10 Ohms $\pm$ 5%.

## Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| $V_{DD}$ | Voltage on $V_{DD}$ pin relative to $V_{SS}$ | - 1.0 V ~ 2.3 V | V | 1 |
| $V_{DDQ}$ | Voltage on $V_{DDQ}$ pin relative to $V_{SS}$ | - 0.5 V ~ 2.3 V | V | 1 |
| $V_{DDL}$ | Voltage on $V_{DDL}$ pin relative to $V_{SS}$ | - 0.5 V ~ 2.3 V | V | 1 |
| $V_{IN}, V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | - 0.5 V ~ 2.3 V | V | 1 |
| $T_{STG}$ | Storage Temperature | -55 to +100 | °C | 1, 2 |

Note :
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.


## AC & DC Operating Conditions

Recommended DC Operating Conditions (SSTL - 1.8)

| Symbol | Parameter | Rating | | | Units | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DD}$ | Supply Voltage | 1.7 | 1.8 | 1.9 | V | |
| $V_{DDL}$ | Supply Voltage for DLL | 1.7 | 1.8 | 1.9 | V | 4 |
| $V_{DDQ}$ | Supply Voltage for Output | 1.7 | 1.8 | 1.9 | V | 4 |
| $V_{REF}$ | Input Reference Voltage | $0.49*V_{DDQ}$ | $0.50*V_{DDQ}$ | $0.51*V_{DDQ}$ | mV | 1,2 |
| $V_{TT}$ | Termination Voltage | $V_{REF}$-0.04 | $V_{REF}$ | $V_{REF}$+0.04 | V | 3 |

Note : There is no specific device $V_{DD}$ supply voltage requirement for SSTL-1.8 compliance. However under all conditions $V_{DDQ}$ must be less than or equal to $V_{DD}$.
1. The value of $V_{REF}$ may be selected by the user to provide optimum noise margin in the system. Typically the value of $V_{REF}$ is expected to be about 0.5 x $V_{DDQ}$ of the transmitting device and $V_{REF}$ is expected to track variations in $V_{DDQ}$.
2. Peak to peak AC noise on $V_{REF}$ may not exceed +/-2% $V_{REF}$(DC).
3. $V_{TT}$ of transmitting device must track $V_{REF}$ of receiving device.
4. AC parameters are measured with $V_{DD}$, $V_{DDQ}$ and $V_{DDL}$ tied together.

## Operating Temperature Condition

| Symbol | Parameter | Rating | Units | Notes |
|--------|-----------|--------|-------|-------|
| TOPER | Operating Temperature | 0 to 95 | °C | 1, 2, 3 |

Note :

1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 0 - 85 °C, operation temperature range are the temperature which all DRAM specification will be supported.
3. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period ( tREFI=3.9 us ) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

## Input DC Logic Level

| Symbol | Parameter | Min. | Max. | Units | Notes |
|--------|-----------|------|------|-------|-------|
| $V_{IH}(DC)$ | DC input logic high | $V_{REF}$ + 0.125 | $V_{DDQ}$ + 0.3 | V | |
| $V_{IL}(DC)$ | DC input logic low | - 0.3 | $V_{REF}$ - 0.125 | V | |

## Input AC Logic Level

| Symbol | Parameter | Min. | Max. | Units | Notes |
|--------|-----------|------|------|-------|-------|
| $V_{IH}(AC)$ | AC input logic high | $V_{REF}$ + 0.250 | - | V | |
| $V_{IL}(AC)$ | AC input logic low | - | $V_{REF}$ - 0.250 | V | |

## AC Input Test Conditions

| Symbol | Condition | Value | Units | Notes |
|--------|-----------|-------|-------|-------|
| $V_{REF}$ | Input reference voltage | $0.5 * V_{DDQ}$ | V | 1 |
| $V_{SWING(MAX)}$ | Input signal maximum peak to peak swing | 1.0 | V | 1 |
| SLEW | Input signal minimum slew rate | 1.0 | V/ns | 2, 3 |

Notes:

1. Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL}(AC)$ level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from $V_{REF}$ to $V_{IH}(AC)$ min for rising edges and the range from $V_{REF}$ to $V_{IL}(AC)$ max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from $V_{IL}(AC)$ to $V_{IH}(AC)$ on the positive transitions and $V_{IH}(AC)$ to $V_{IL}(AC)$ on the negative transitions.

< AC Input Test Signal Waveform >

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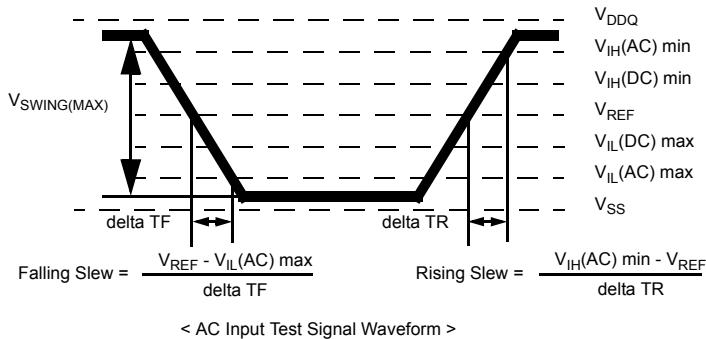
## IDD Specification Parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

| Symbol | Proposed Conditions | | Units | Notes |
|---|---|---|---|---|
| IDD0 | **Operating one bank active-precharge current**;<br>$t$CK = $t$CK(IDD), $t$RC = $t$RC(IDD), $t$RAS = $t$RASmin(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA | |
| IDD1 | **Operating one bank active-read-precharge current**;<br>IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t$CK = $t$CK(IDD), $t$RC = $t$RC (IDD), $t$RAS = $t$RASmin(IDD), $t$RCD = $t$RCD(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | | mA | |
| IDD2P | **Precharge power-down current**;<br>All banks idle; $t$CK = $t$CK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | | mA | |
| IDD2Q | **Precharge quiet standby current**;<br>All banks idle; $t$CK = $t$CK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | | mA | |
| IDD2N | **Precharge standby current**;<br>All banks idle; $t$CK = $t$CK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA | |
| IDD3P | **Active power-down current**;<br>All banks open; $t$CK = $t$CK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | Fast PDN Exit MRS(12) = 0mA | mA | |
| | | Slow PDN Exit MRS(12) = 1mA | mA | |
| IDD3N | **Active standby current**;<br>All banks open; $t$CK = $t$CK(IDD), $t$RAS = $t$RASmax(IDD), $t$RP = $t$RP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA | |
| IDD4W | **Operating burst write current**;<br>All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t$CK = $t$CK(IDD), $t$RAS = $t$RASmax(IDD), $t$RP = $t$RP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA | |
| IDD4R | **Operating burst read current**;<br>All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t$CK = $t$CK(IDD), $t$RAS = $t$RASmax(IDD), $t$RP = $t$RP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | | mA | |
| IDD5B | **Burst auto refresh current**;<br>$t$CK = $t$CK(IDD); Refresh command at every $t$RFC(IDD) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA | |
| IDD6 | **Self refresh current**;<br>CK and CK\ at 0V; CKE $\leq$ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING | Normal | mA | |
| | | Low Power | mA | |
| IDD7 | **Operating bank interleave read current**;<br>All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $t$RCD(IDD)-1*$t$CK(IDD); $t$CK = $t$CK(IDD), $t$RC = $t$RC(IDD), $t$RRD = $t$RRD(IDD), $t$FAW = $t$FAW(IDD), $t$RCD = 1*$t$CK(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions | | mA | |

## Operating Current Table(1-1) (T$_A$=0ºC, VDD= 1.9V)

### M470T6554BG(Z)3/M470T6554BG(Z)0 : 64Mx64 512MB Module

| Symbol | CD5 (DDR533@CL=4) | LD5 (DDR533@CL=4) | CCC (DDR400@CL=3) | LCC (DDR400@CL=3) | Unit | Notes |
|---|---|---|---|---|---|---|
| IDD0 | 760 | 460 | 720 | 460 | mA | |
| IDD1 | 860 | 560 | 760 | 520 | mA | |
| IDD2P | 64 | 64 | 64 | 64 | mA | |
| IDD2Q | 200 | 200 | 200 | 200 | mA | |
| IDD2N | 240 | 200 | 240 | 200 | mA | |
| IDD3P-F | 240 | 120 | 240 | 120 | mA | |
| IDD3P-S | 120 | 120 | 120 | 120 | mA | |
| IDD3N | 560 | 260 | 520 | 260 | mA | |
| IDD4W | 1,200 | 700 | 1,000 | 700 | mA | |
| IDD4R | 1,100 | 700 | 940 | 700 | mA | |
| IDD5B | 1,060 | 860 | 1,000 | 860 | mA | |
| IDD6 | 44 | 40 | 44 | 40 | mA | |
| IDD7 | 1,840 | 1,060 | 1,760 | 1,060 | mA | |

* Module IDD  was calculated on the basis of component IDD and  can be differently measured  according to DQ loading cap.

### M470T3354BG(Z)3/M470T3354BG(Z)0 : 32Mx64 256MB Module

| Symbol | CD5 (DDR533@CL=4) | LD5 (DDR533@CL=4) | CCC (DDR400@CL=3) | LCC (DDR400@CL=3) | Unit | Notes |
|---|---|---|---|---|---|---|
| IDD0 | 480 | 360 | 460 | 360 | mA | |
| IDD1 | 580 | 460 | 500 | 420 | mA | |
| IDD2P | 32 | 32 | 32 | 32 | mA | |
| IDD2Q | 100 | 100 | 100 | 100 | mA | |
| IDD2N | 120 | 100 | 120 | 100 | mA | |
| IDD3P-F | 120 | 60 | 120 | 60 | mA | |
| IDD3P-S | 60 | 60 | 60 | 60 | mA | |
| IDD3N | 280 | 160 | 260 | 160 | mA | |
| IDD4W | 920 | 600 | 740 | 520 | mA | |
| IDD4R | 820 | 600 | 680 | 520 | mA | |
| IDD5B | 780 | 760 | 740 | 760 | mA | |
| IDD6 | 22 | 20 | 22 | 20 | mA | |
| IDD7 | 1,560 | 960 | 1,500 | 960 | mA | |

* Module IDD  was calculated on the basis of component IDD and  can be differently measured  according to DQ loading cap.

## Operating Current Table(1-2) $(T_A=0^oC, V_{DD}= 1.9V)$

**M470T2953BS(Y)3/M470T2953BS(Y)0 : 128Mx64 1GB Module**

| Symbol | CD5 (DDR533@CL=4) | LD5 (DDR533@CL=4) | CCC (DDR400@CL=3) | LCC (DDR400@CL=3) | Unit | Notes |
|--------|------|------|------|------|------|-------|
| IDD0 | 1,360 | 760 | 1,280 | 760 | mA | |
| IDD1 | 1,440 | 920 | 1,320 | 840 | mA | |
| IDD2P | 128 | 128 | 128 | 128 | mA | |
| IDD2Q | 400 | 400 | 400 | 400 | mA | |
| IDD2N | 480 | 400 | 480 | 400 | mA | |
| IDD3P-F | 480 | 240 | 480 | 240 | mA | |
| IDD3P-S | 240 | 240 | 240 | 240 | mA | |
| IDD3N | 1,120 | 520 | 1,040 | 520 | mA | |
| IDD4W | 2,160 | 1,160 | 1,680 | 1,000 | mA | |
| IDD4R | 2,000 | 1,160 | 1,680 | 1,000 | mA | |
| IDD5B | 2,120 | 1,720 | 2,000 | 1,720 | mA | |
| IDD6 | 88 | 80 | 88 | 80 | mA | |
| IDD7 | 2,760 | 1,960 | 2,680 | 1,960 | mA | |

\* Module IDD  was calculated on the basis of component IDD and  can be differently measured  according to DQ loading cap.

## Input/Output Capacitance $(V_{DD}=1.8V, V_{DDQ}=1.8V, T_A=25^oC)$

| Parameter / Non-ECC | Symbol | Min M470T6554BG(Z)3 M470T6554BG(Z)0 | Max | Min M470T3354BG(Z)3 M470T3354BG(Z)0 | Max | Min M470T2953BS(Y)3 M470T2953BS(Y)0 | Max | Units |
|---------------------|--------|-----|-----|-----|-----|-----|-----|-------|
| Input capacitance, CK and $\overline{CK}$ | CCK | - | 32 | - | 24 | - | 48 | |
| Input capacitance, CKE , $\overline{CS}$, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | CI | - | 34 | - | 34 | - | 42 | pF |
| Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$ | CIO | - | 10 | - | 6 | - | 10 | |

\* DM is internally loaded to match DQ and DQS identically.

## Electrical Characteristics & AC Timing for DDR2-533/400 SDRAM

(0 °C $\leq$ T$_{CASE}$ $\leq$ 95 °C; V$_{DDQ}$ = 1.8V $\pm$ 0.1V; V$_{DD}$ = 1.8V $\pm$ 0.1V)

### Refresh Parameters by Device Density

| Parameter | Symbol | | 256Mb | 512Mb | 1Gb | 2Gb | 4Gb | Units |
|---|---|---|---|---|---|---|---|---|
| Refresh to active/Refresh command time | tRFC | | 75 | 105 | 127.5 | 195 | tbd | ns |
| Average periodic refresh interval | tREFI | 0 °C $\leq$ T$_{CASE}$ $\leq$ 85°C | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | $\mu$s |
| | | 85 °C $<$ T$_{CASE}$ $\leq$ 95°C | 3.9 | 3.9 | 3.9 | 3.9 | 3.9 | $\mu$s |

### Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

| Speed | DDR2-533(D5) | | DDR2-400(CC) | | Units |
|---|---|---|---|---|---|
| Bin (CL - tRCD - tRP) | 4 - 4 - 4 | | 3 - 3 - 3 | | |
| Parameter | min | max | min | max | |
| tCK, CL=3 | 5 | 8 | 5 | 8 | ns |
| tCK, CL=4 | 3.75 | 8 | 5 | 8 | ns |
| tCK, CL=5 | - | - | - | - | ns |
| tRCD | 15 | | 15 | | ns |
| tRP | 15 | | 15 | | ns |
| tRC | 55 | | 55 | | ns |
| tRAS | 40 | 70000 | 40 | 70000 | ns |

## Timing Parameters by Speed Grade

(Refer to notes for informations related to this table at the bottom)

| Parameter | Symbol | DDR2-533 min | DDR2-533 max | DDR2-400 min | DDR2-400 max | Units | Notes |
|---|---|---|---|---|---|---|---|
| DQ output access time from CK/$\overline{CK}$ | tAC | -500 | +500 | -600 | +600 | ps | |
| DQS output access time from CK/$\overline{CK}$ | tDQSCK | -450 | +450 | -500 | +500 | ps | |
| CK high-level width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK low-level width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK half period | tHP | min(tCL, tCH) | x | min(tCL, tCH) | x | ps | |
| Clock cycle time, CL=x | tCK | 3750 | 8000 | 5000 | 8000 | ps | |
| DQ and DM input hold time | tDH | 225 | x | 275 | x | ps | |
| DQ and DM input setup time | tDS | 100 | x | 150 | x | ps | |
| Control & Address input pulse width for each input | tIPW | 0.6 | x | 0.6 | x | tCK | |
| DQ and DM input pulse width for each input | tDIPW | 0.35 | x | 0.35 | x | tCK | |
| Data-out high-impedance time from CK/$\overline{CK}$ | tHZ | x | tAC max | x | tAC max | ps | |
| DQS low-impedance time from CK/$\overline{CK}$ | tLZ(DQS) | tAC min | tAC max | tAC min | tAC max | ps | |
| DQ low-impedance time from CK/$\overline{CK}$ | tLZ(DQ) | 2* tACmin | tAC max | 2* tACmin | tAC max | ps | |
| DQS-DQ skew for DQS and associated DQ signals | tDQSQ | x | 300 | x | 350 | ps | |
| DQ hold skew factor | tQHS | x | 400 | x | 450 | ps | |
| DQ/DQS output hold time from DQS | tQH | tHP - tQHS | x | tHP - tQHS | x | ps | |
| Write command to first DQS latching transition | tDQSS | WL-0.25 | WL+0.25 | WL-0.25 | WL+0.25 | tCK | |
| DQS input high pulse width | tDQSH | 0.35 | x | 0.35 | x | tCK | |
| DQS input low pulse width | tDQSL | 0.35 | x | 0.35 | x | tCK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | x | 0.2 | x | tCK | |
| DQS falling edge hold time from CK | tDSH | 0.2 | x | 0.2 | x | tCK | |
| Mode register set command cycle time | tMRD | 2 | x | 2 | x | tCK | |
| Write postamble | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| Write preamble | tWPRE | 0.35 | x | 0.35 | x | tCK | |
| Address and control input hold time | tIH | 375 | x | 475 | x | ps | |
| Address and control input setup time | tIS | 250 | x | 350 | x | ps | |
| Read preamble | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | tCK | |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| Active to active command period for 1KB page size products | tRRD | 7.5 | x | 7.5 | x | ns | |
| Active to active command period for 2KB page size products | tRRD | 10 | x | 10 | x | ns | |
| Four Activate Window for 1KB page size products | tFAW | 37.5 | | 37.5 | | ns | |
| Four Activate Window for 2KB page size products | tFAW | 50 | | 50 | | ns | |
| $\overline{CAS}$ to $\overline{CAS}$ command delay | tCCD | 2 | | 2 | | tCK | |
| Write recovery time | tWR | 15 | x | 15 | x | ns | |
| Auto precharge write recovery + precharge time | tDAL | tWR+tRP | x | tWR+tRP | x | tCK | |
| Internal write to read command delay | tWTR | 7.5 | x | 10 | x | ns | |
| Internal read to precharge command delay | tRTP | 7.5 | | 7.5 | | ns | |
| Exit self refresh to a non-read command | tXSNR | tRFC + 10 | | tRFC + 10 | | ns | |
| Exit self refresh to a read command | tXSRD | 200 | | 200 | | tCK | |
| Exit precharge power down to any non-read command | tXP | 2 | x | 2 | x | tCK | |
| Exit active power down to read command | tXARD | 2 | x | 2 | x | tCK | |
| Exit active power down to read command (Slow exit, Lower power) | tXARDS | 6 - AL | | 6 - AL | | tCK | |

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| Parameter | Symbol | DDR2-533 | | DDR2-400 | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | min | max | min | max | | |
| CKE minimum pulse width (high and low pulse width) | tCKE | 3 | | 3 | | tCK | |
| ODT turn-on delay | tAOND | 2 | 2 | 2 | 2 | tCK | |
| ODT turn-on | tAON | tAC(min) | tAC(max)+1 | tAC(min) | tAC(max)+1 | ns | |
| ODT turn-on(Power-Down mode) | tAONPD | tAC(min)+2 | 2tCK+tAC(max)+1 | tAC(min)+2 | 2tCK+tAC(max)+1 | ns | |
| ODT turn-off delay | tAOFD | 2.5 | 2.5 | 2.5 | 2.5 | tCK | |
| ODT turn-off | tAOF | tAC(min) | tAC(max)+0.6 | tAC(min) | tAC(max)+0.6 | ns | |
| ODT turn-off (Power-Down mode) | tAOFPD | tAC(min)+2 | 2.5tCK+tAC(max)+1 | tAC(min)+2 | 2.5tCK+tAC(max)+1 | ns | |
| ODT to power down entry latency | tANPD | 3 | | 3 | | tCK | |
| ODT power down exit latency | tAXPD | 8 | | 8 | | tCK | |
| OCD drive mode output delay | tOIT | 0 | 12 | 0 | 12 | ns | |
| Minimum time clocks remains ON after CKE asynchronously drops LOW | tDelay | tIS+tCK +tIH | | tIS+tCK +tIH | | ns | |

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## Physical Dimensions: 32Mbx16 based 64Mx64 Module(2 Rank)
### M470T6554BG(Z)3/M470T6554BG(Z)0
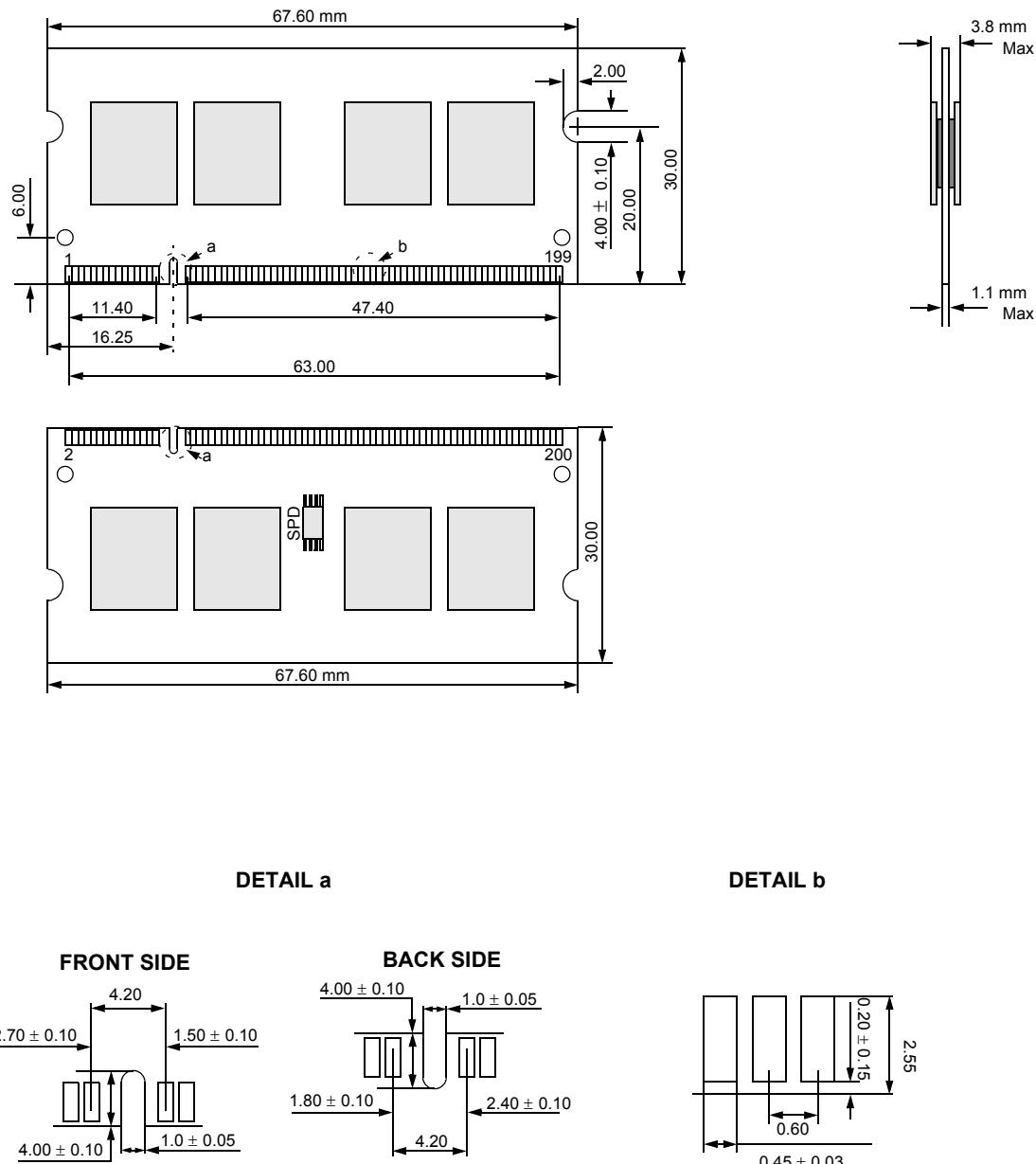


**DETAIL a**

**DETAIL b**

**FRONT SIDE**

**BACK SIDE**

The used device is 32M x16 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T51163QB

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## Physical Dimensions: 32Mbx16 based 32Mx64 Module(1 Rank)
### M470T3354BG(Z)3/M470T3354BG(Z)0
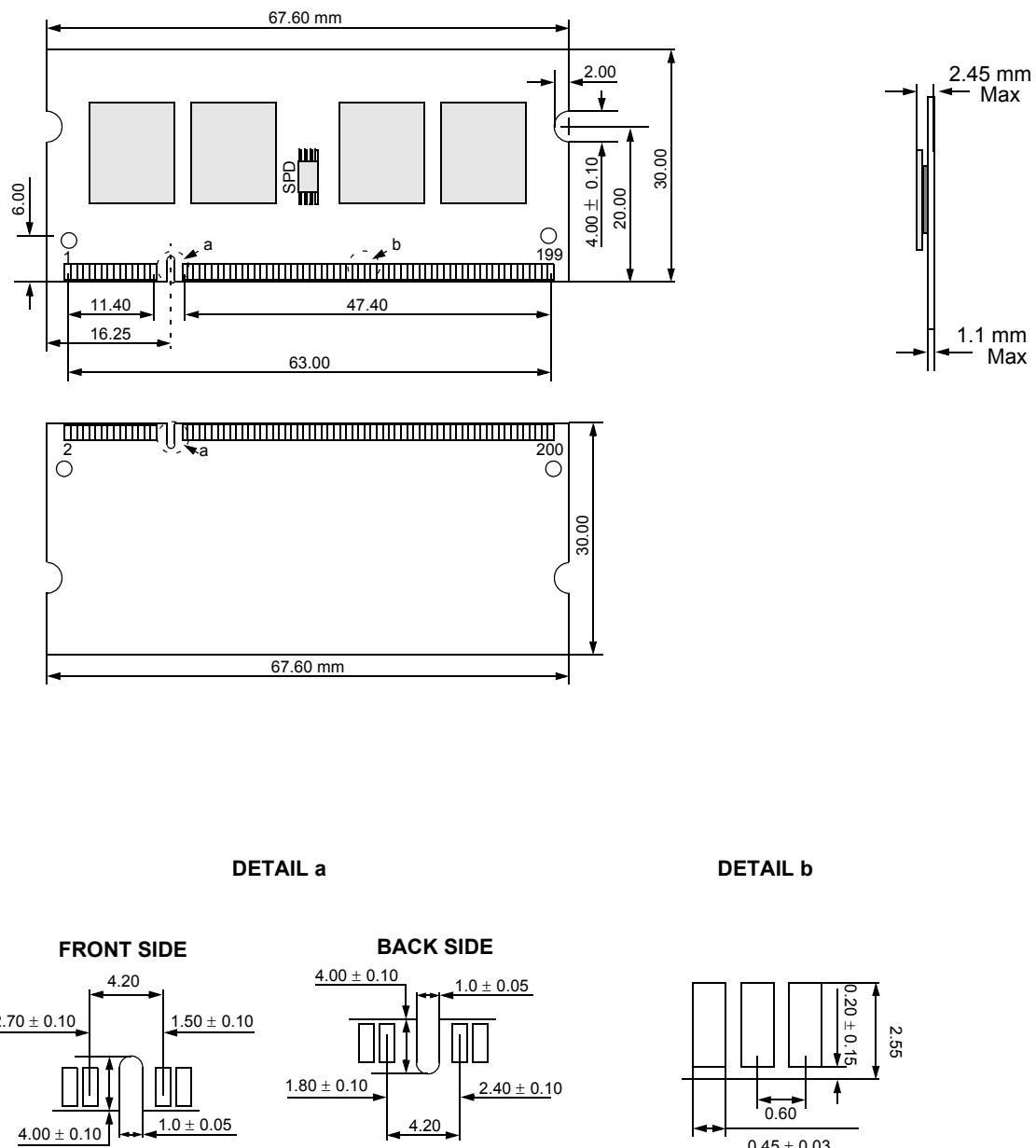


**DETAIL a**

**DETAIL b**

**FRONT SIDE**

**BACK SIDE**

The used device is 32M x16 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T51163QB

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## Physical Dimensions: 64Mbx8 based 128Mx64 Module(2 Ranks)
### M470T2953BS(Y)3/M470T2953BS(Y)0



**DETAIL a**

**DETAIL b**

**FRONT SIDE**

**BACK SIDE**
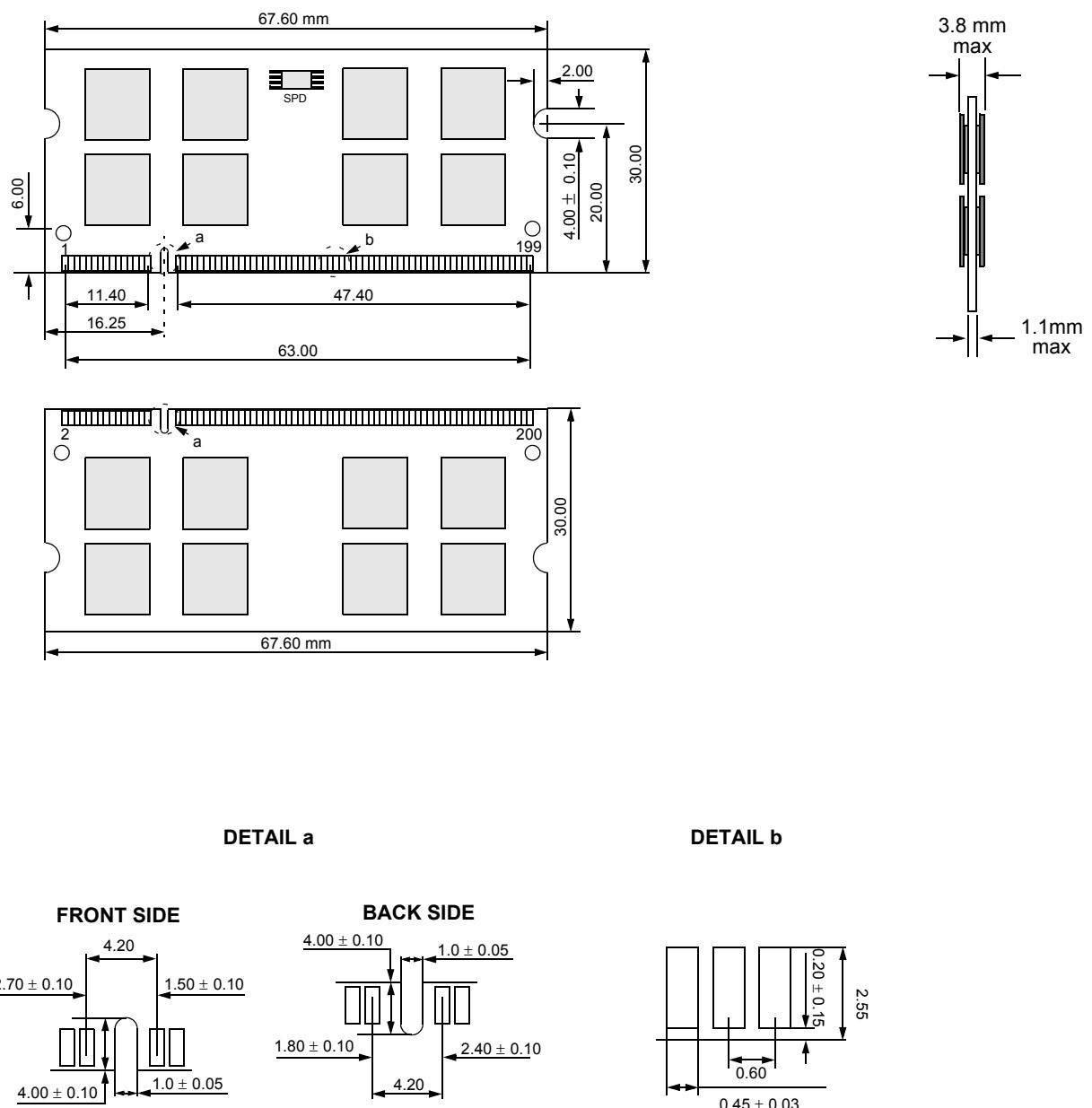
The used device is 64M x8 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T51083QB

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## Revision History

**Revision 1.0 (Jan. 2004)**
 - Initial Release

**Revision 1.1 (Jun. 2004)**
 - Added lead-free part number in the ordering information
 - Changed IDD2P

**Revision 1.2 (Jul. 2004)**

 - Added current values and part number of low power product

**Revision 1.3 (Feb. 2005)**
 - Added the detail information for mechanical dimension

**Revision 1.4 (Mar. 2005)**
 - Changed 1GB Functional Block Diagram

**Revision 1.5 (Aug. 2005)**
 - Changed the IDD Specification Parameters Definition

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